FIG.1 PRIOR ART

BLOCK DIAGRAM SHOWING CONFIGURATION OF CONVENTONAL CLOCK
CLOCK MULTIPLYING PLL CIRCUIT

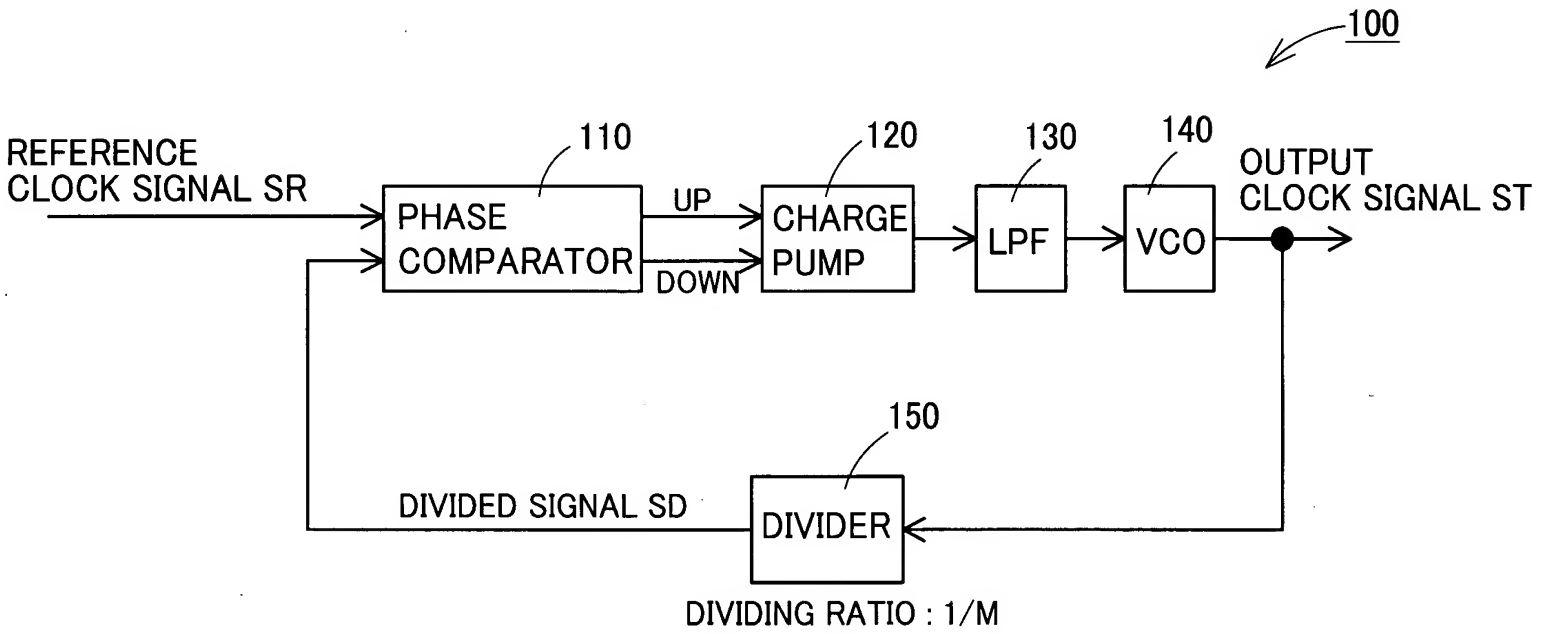

FIG.2

BLOCK DIAGRAM ILLUSTRATING SCHEMATIC CONFIGURATION OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT

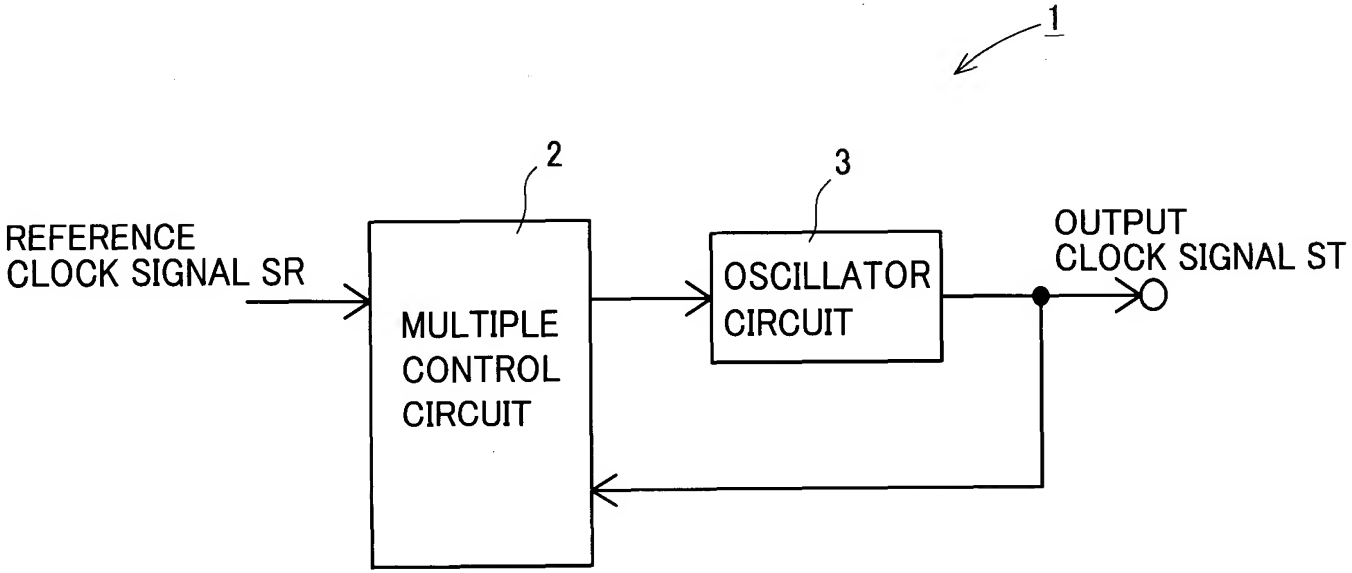

FIG.3

BLOCK DIAGRAM DEPICTING CONFIGURATION OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT

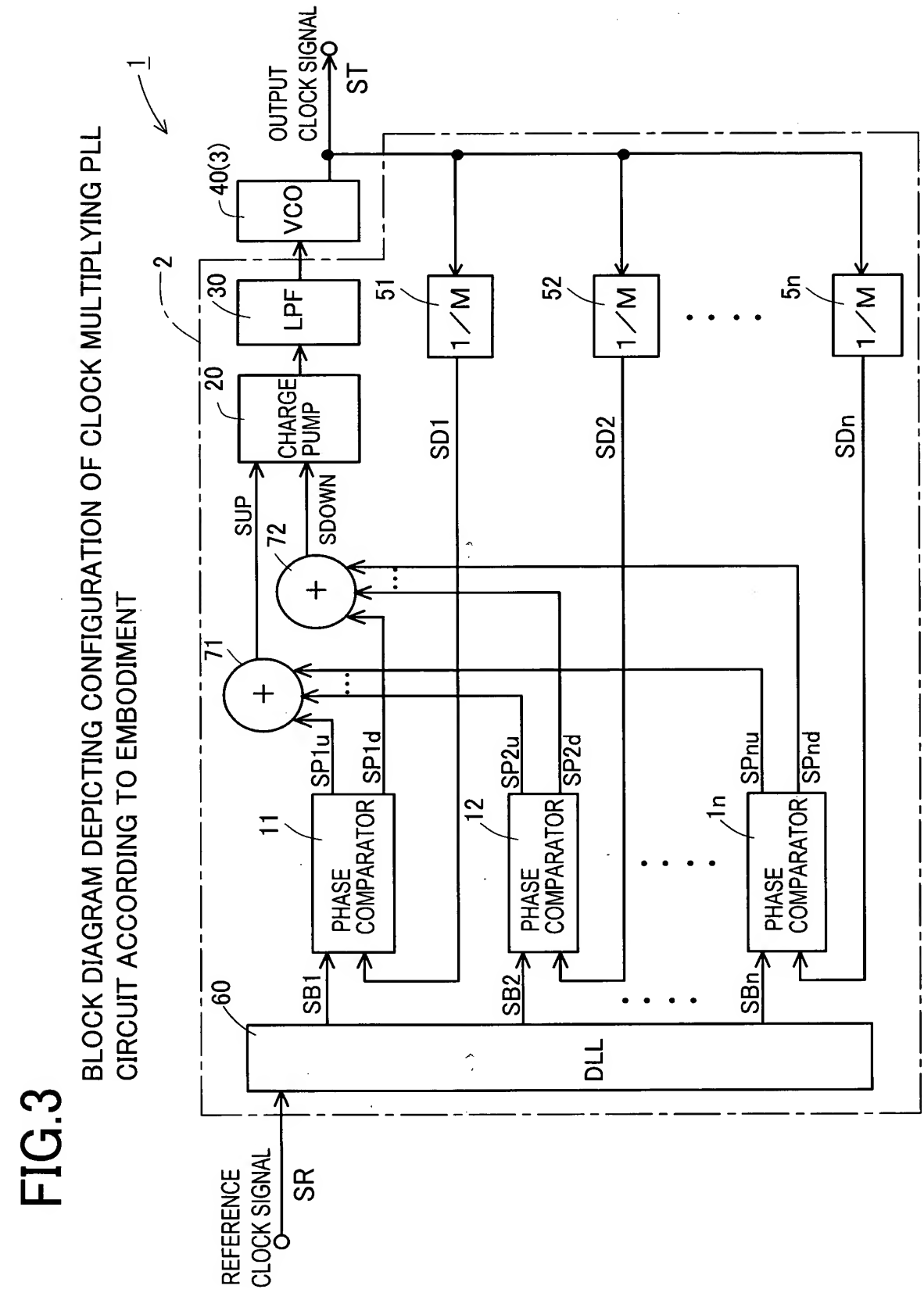

FIG.4

TIME CHART SHOWING CHANGES IN FIRST THROUGH n-th REFERENCE CLOCK SIGNAL

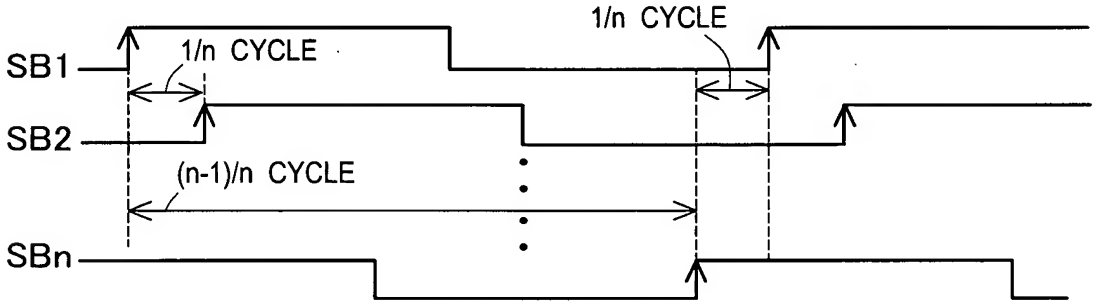

FIG.5

TIME CHART ILLUSTRATING CHANGES IN FIRST THROUGH n-th DIVIDED SIGNAL

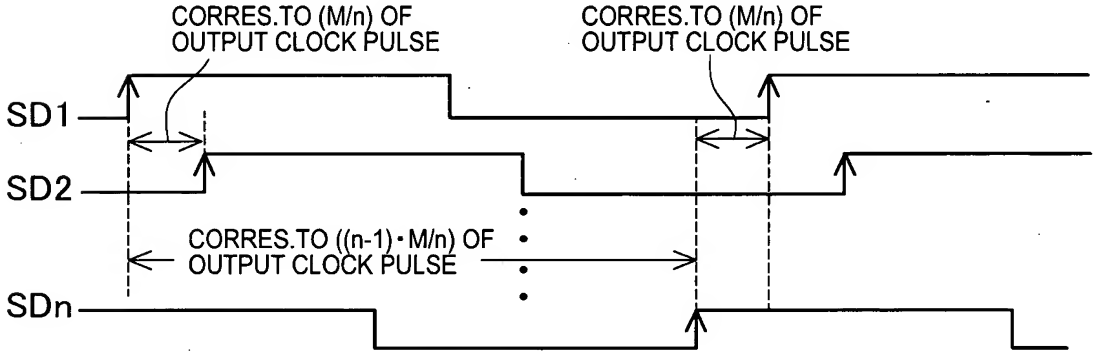

FIG.6

TIME CHART RELATED TO PHASE COMPARISONS OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT

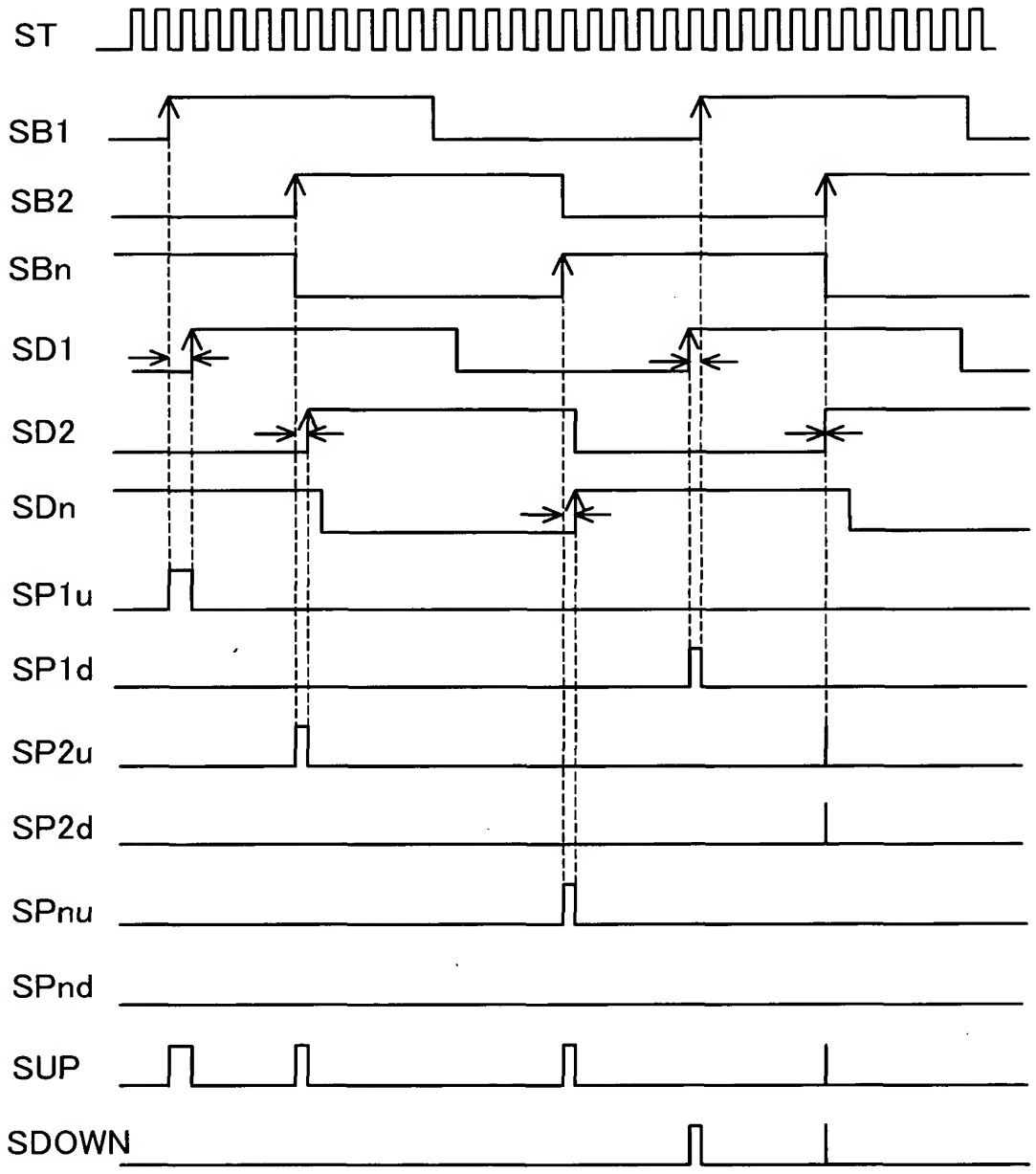

FIG.7

BLOCK DIAGRAM OF CONFIGURATION OF CLOCK MULTIPLYING PLL CIRCUIT ACCORDING TO EMBODIMENT AND INCLUDING DIVIDER INITIAL RESET MEANS